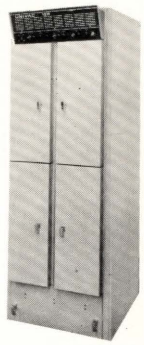
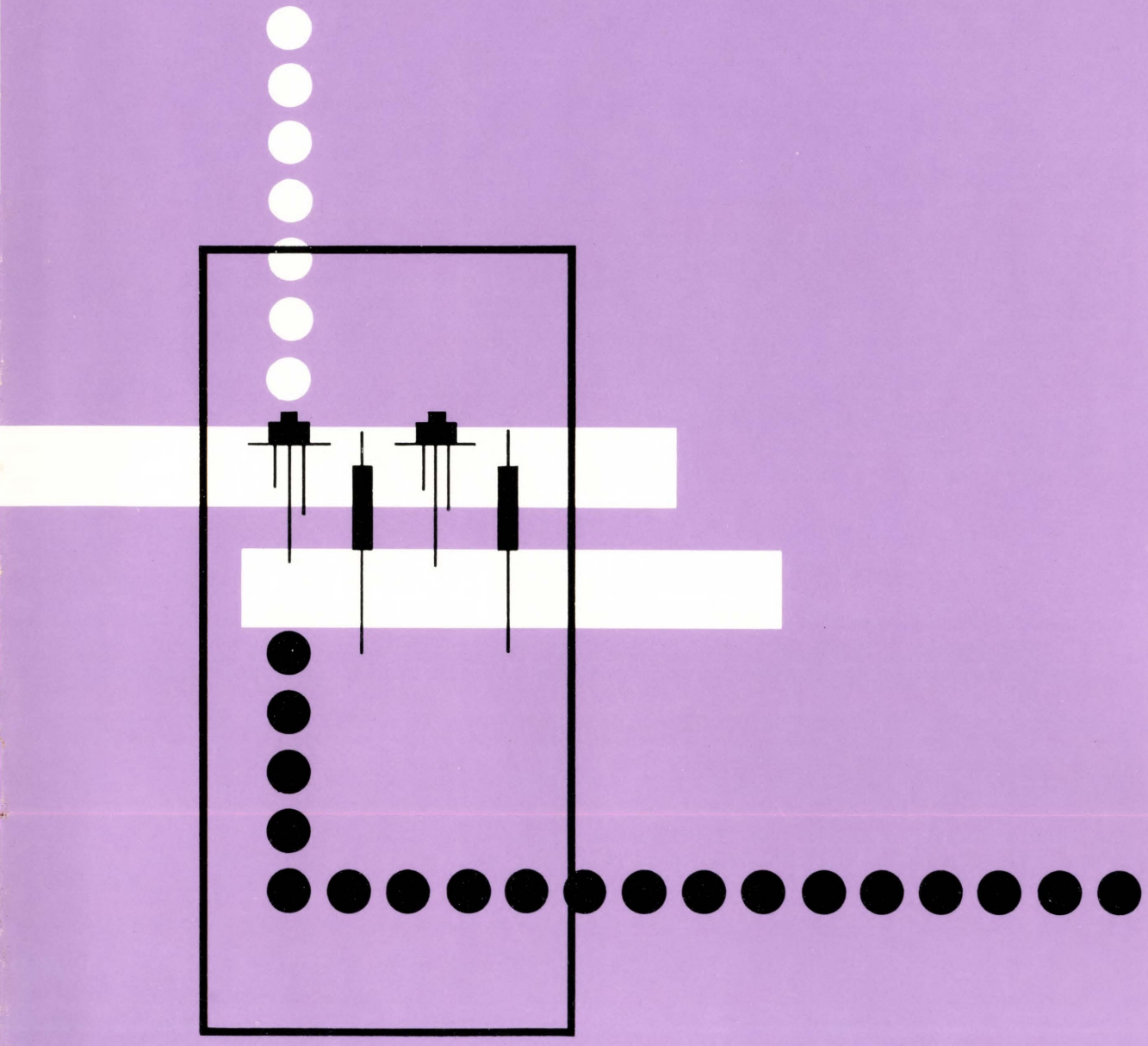
UNIVAC® 1219

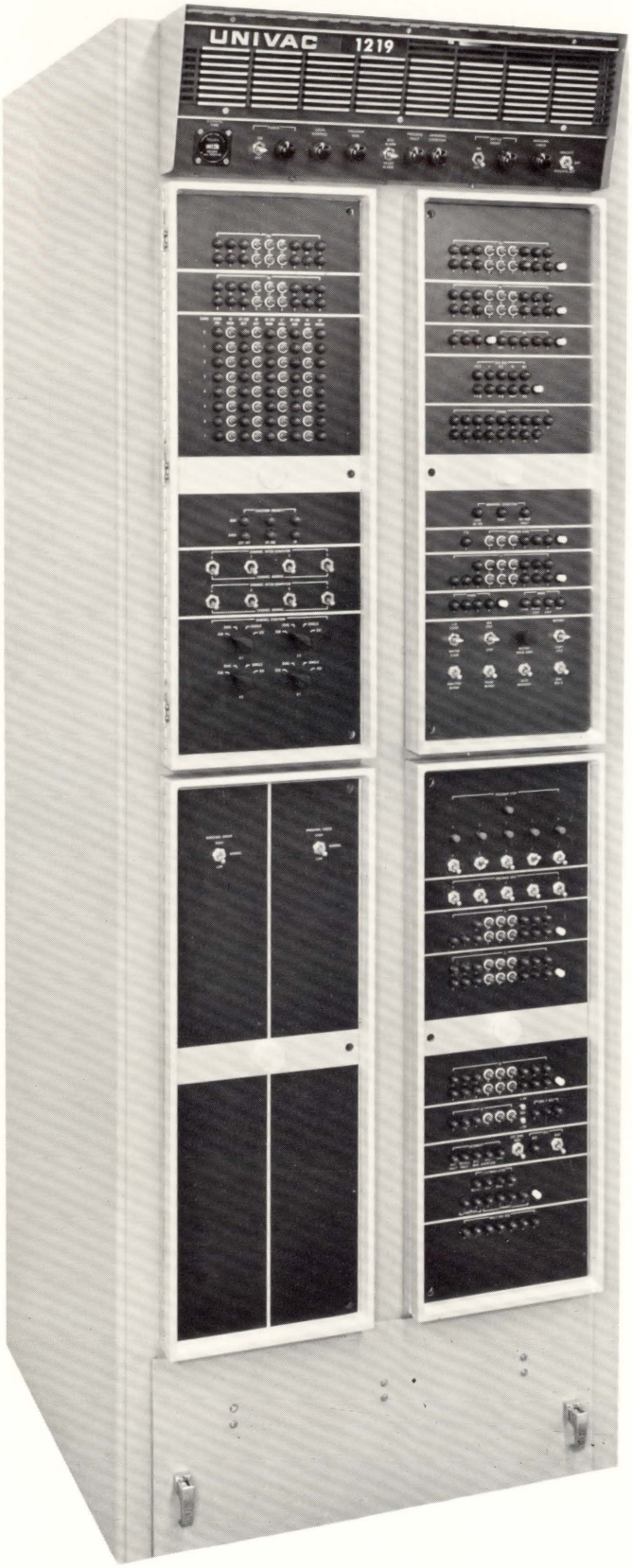
MILITARY COMPUTER



GENERAL DESCRIPTION



UNIVAC 1219 COMPUTER



UNIVAC
DEFENSE SYSTEMS DIVISION
5316 W. IMPERIAL HWY.
LOS ANGELES, CALIF. 90045
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UNIVAC 1219 COMPUTER

GENERAL

The UNIVAC® 1219 Computer is a medium scale, general-purpose computer. It is a faster version of the widely-used UNIVAC 1218 Computer and is functionally compatible with it. It is an advanced military computer designed to comply with the environmental specifications of MIL-E-16400.

The UNIVAC 1219 Computer is an 18-bit digital computer capable of transferring 500,000 words per second. The computer is capable of processing large quantities of data in a real-time application. Arithmetic and input/output operations can be performed on the basis of a single length 18-bit word or a double length 36-bit word, if required for greater precision or for compatibility with other computers. It is equipped with a 2-microsecond Main Memory and features a 500-nanosecond Control Memory. It can be supplied with 16 full-duplex I/O channels where each channel is associated with a complete set of program interrupts. It is equipped with an external synchronizer function in addition to an automatic addressable clock cell. The UNIVAC 1219 Computer has been designed to provide a complete, straightforward interface enabling easy adaption to the requirements of a system rather than requiring modification of the system to accommodate the computer.

SPECIAL FEATURES

Real-Time Processing

The ability of the UNIVAC 1219 Computer to process various applications concurrently is implemented by a program intervention system called "Interrupts". These Interrupts may originate at some remote external device (External Interrupts) or they may originate within the computer (Internal Interrupts). Since more than one may occur at the same time, the computer possesses a priority scheme with decision-making qualities so that it can select the branch of operation for solving the problem requiring the most urgent attention. Under program control, the other interrupts may be honored in turn according to the next highest priority or they may be ignored. With this "interrupt" feature, real-time problem solution and maximum processing potential of the system is realized since less important routines can occupy the computer's surplus time.

Continuous Data Mode (CDM)

The Continuous Data Mode, requested when initiating a buffer on a channel, is a feature which provides an automatic reinitiation of the buffer upon completion. A new pair of buffer control words are transferred to the control memory buffer control addresses from the control memory CDM addresses for that channel. The Monitor Interrupt can be incorporated with the CDM and if so, the interrupt will occur each time the buffer is terminated and reinitiated. The CDM is especially useful when a continuous, high rate, stream of data must be transferred in or out of the computer.

Intercomputer Time Out Interrupt

The Intercomputer Time Out Interrupt is available during intercomputer operation. Any single bit of the RTC incrementing register may be wired to monitor the Resume circuitry. When the RTC count reaches the specified bit, a designator is set. If no Resume is received by the computer before the next time the count reaches that bit, the intercomputer time out interrupt is activated and the next program instruction is taken for the IC Interrupt Entrance Register.

Externally Specified Index (ESI)

This outstanding feature provides peripheral devices with a means of specifying core storage areas in the computer's memory for any input or output transfers they may request. The Externally Specified Index (ESI) mode of operation is useful as a multiplexing device for a number of slow transfer peripheral units occupying one dual channel. The buffer control words governing the transfers are located at the INDEX address. If input is desired, an Input Request is presented with the Index on one channel of the pair and the data on the other channel. If Output is desired, an Output Request is presented with the Index address.

Externally Specified Addressing (ESA)

The ESA feature provides peripheral devices with a means of specifying an absolute core memory location for storage or retrieval of data. An active dual-channel mode of operation is required for computer response to this function. The address is presented on one channel and the data transmission path on the other. If input is desired, the external device presents an Input Request with the address and data. If output is desired, an Output Request is presented with the address.

Main Memory and Control Memory Concurrent Operation

The Master clock in the UNIVAC 1219 Computer

controls and synchronizes all operations performed by the various sections through the electronic timing chains allotted to them. The read/restore cycle time of main memory is 2-microseconds. All control and timing sequences for the various functions the computer performs are based on this 2-microsecond cycle. Four 500-nanosecond control memory read-write cycles occur during one main memory read-write cycle. An instruction from main memory storage can be transferred to the control section for execution in approximately 0.9 microseconds. Any modification to this instruction and complete translation is completed before the end of that main memory cycle since the modifiers are extracted from control memory in less than 250 nanoseconds. The Input/Output section has independent access to control memory for its control words, clocks, etc., during instruction sequences.

SYSTEM INTERFACE

The UNIVAC 1219 Computer can be used with a large variety of local or remote peripheral devices as an independent complete general-purpose system, or it can operate as a satellite pre-processor with larger systems to supply off-line, or associated on-line operations. Twenty-one program instructions are devoted to the control of Input/Output, providing positive control and a high degree of sophistication in programming. Among the peripheral devices available for use with the 1219 are the following:

- Input/Output Console—provides a paper tape reader (300 cps), paper tape punch (110 cps), and alpha/numeric keyboard and page printer
- Magnetic Tape Systems—compatible with 200, 556, and 800 bpi systems at up to 120K characters/second
- High Speed Line Printer—provides alpha numeric printing 120 character lines
- Communications Units —provide data handling capabilities for telegraph or telephone line bit rates
- Magnetic Drum Storage—use with FH330, FH880, and FASTRAND drum; drums can be multiplexed

Other Input/Output devices are available to meet standard or special requirements.

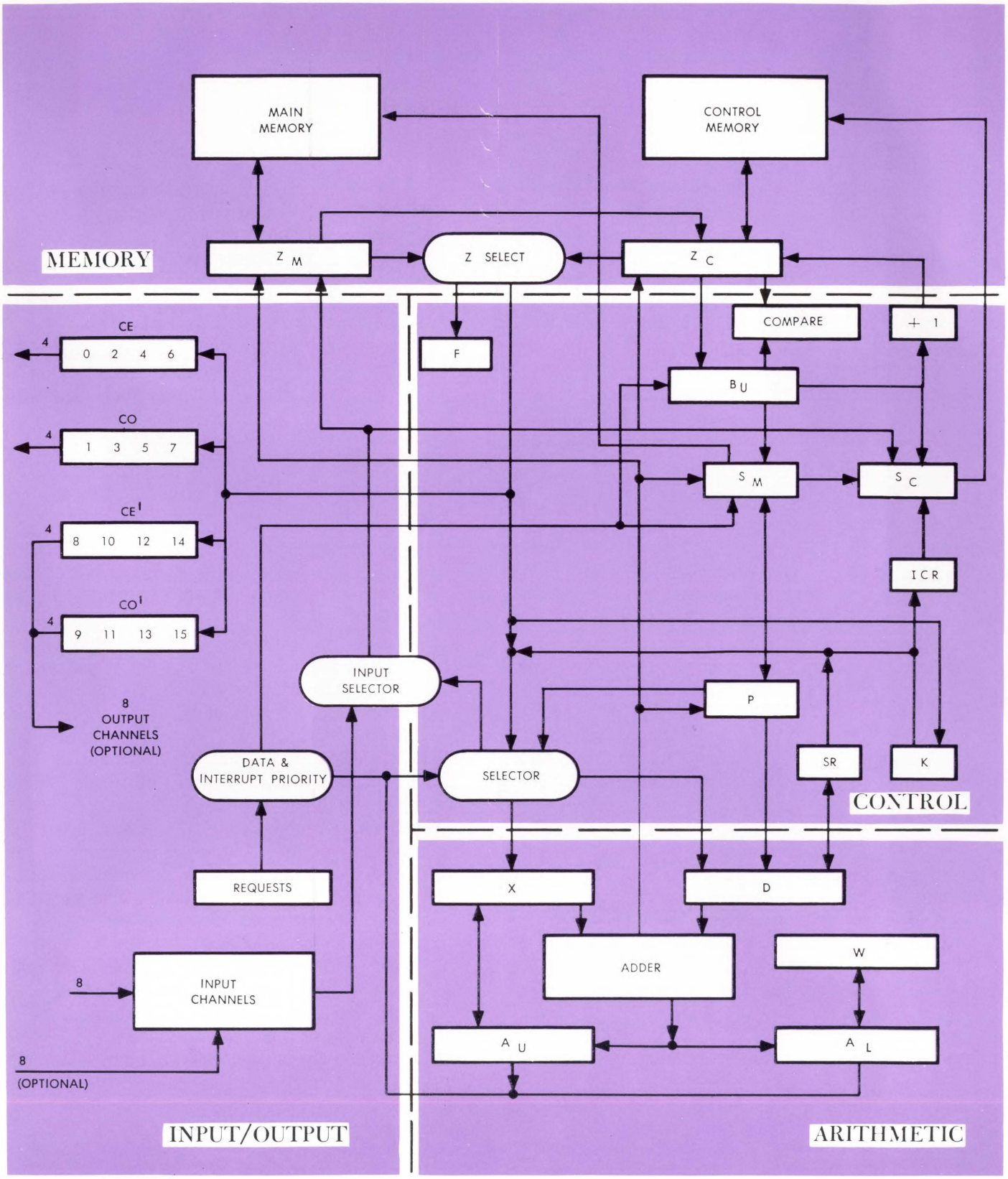
COMPUTER MAINTAINABILITY

Maintainability is enhanced by the mechanical design which provides front access to repair or replace printed circuit modules. Other equally important features include the front panel display of all registers, manual alteration of all registers, and switches for operation stepping, sequence stepping, or phase stepping, at a manually controlled variable clock speed. Test points from important circuit areas are available at test blocks on the front panels. Because the computer uses low-voltage, solid-state components of proven life and reliability, it is compact and dependable. Only minimum site preparation and maintenance are required.

SUPPORTING SERVICES

UNIVAC support of 1219 Computer systems includes assistance in the following areas:

- System Analysis—Total capability of a highly competent staff is available to users for problem analysis, equipment specification, mathematical modeling, or operational support for any application.
- Programming—In addition to the software package supplied with the computer (i.e., a mnemonic assembler, polycode assembler, floating point package, function evaluation sub-routines, and program debugging aids, etc.) experienced, skilled programmers are available to assist customers to obtain maximum performance from the UNIVAC 1219 Computer.
- Maintenance—The UNIVAC Field Engineering Department, a complete support organization made up of fully-trained field engineers, provides spare parts and service throughout the world. This support begins with site planning and preparation and continues throughout installation, checkout, and normal operation, as required.
- Training—A staff of well-trained instructors is available for conducting training courses for customer personnel. Classes covering programming, operation, and maintenance of all equipment can be provided at UNIVAC or at the customer's facility.



UNIVAC 1219 COMPUTER BLOCK DIAGRAM

TECHNICAL CHARACTERISTICS

MEMORY

Control Memory

Cycle Time:	500 nanoseconds
Capacity:	128 or 256 18-bit words
Type:	Word organized, magnetic core
Purpose:	Index registers, clock cells, I/O buffer control registers; operates in the "shadow" of the Main Memory at a 4:1 ratio.

Main Memory

Cycle Time:	2 microseconds
Capacity:	8192, 16,384, 32,768 or 65,536 18-bit words (standard options)
Type:	Coincident current, magnetic core
Purpose:	I/O interrupt registers, program and data storage.

Nondestructive Readout Memory

Cycle Time:	2 microseconds
Capacity:	32 18-bit words
Type:	Word organized, transformer core, unalterable
Purpose:	Bootstrap (initial load) program storage. Programs available for paper tape and magnetic tape load; others on request.

INPUT/OUTPUT

Channels

Type:	Simplex, 18-bit parallel
Number:	32 maximum; 16 input plus 16 output
Transfer Rate:	One channel—166,000 18-bit words per second (maximum) Multi-channel—500,000 18-bit words per second (maximum)
Operation:	Each channel fully buffered and once activated operates without program attention, asynchronously, at the rate of the peripheral unit.

Information Transfers

Input Channels:	Input data, interrupt data
Output Channels:	Output data, external command data
Processing Time Required:	2 microseconds/word transferred 0 microsecond during extended sequence instructions
Delay due to Program:	2 microseconds (maximum)

Operating Modes (Standard)

Normal Single Channel:
18-bit parallel transfers

Normal Dual Channel:
Consecutive (even/odd numbered) channels may be "paired" to form a single 36-bit parallel channel.

Externally Specified Index (Dual Channel):
18-bit parallel data transfers with storage address indirectly specified by external device; useful for multiplexing/decommutating data to/from computer.

Externally Specified Address (Dual Channel):
18-bit parallel data transfers with storage address directly specified by external device.

Continuous Data Mode:
Program controlled automatic reinitiation of previously established buffers. Program controlled termination of CDM. 18-bit parallel or 36-bit parallel input/output word transfers.

Intercomputer Single Channel:
Direct 18-bit parallel data transfers with other UNIVAC computers. No interface adapters required for intercomputer communication.

Intercomputer Dual Channel:
Direct 36-bit parallel data transfer with other UNIVAC computers. No interface adapters required for intercomputer communication.

Interrupts

Input Channels:
16 external interrupts plus 16 internal interrupts (programmer option)

Output Channels:
16 internal interrupts (programmer option)

CONTROL

Instructions
- Single Address
- Address Modification: 8 Control-Memory contained index registers
- Repertoire: 102 instructions

Clock
- Type: Automatic, additive, under program control
- Location: Control Memory
- Duration: Established under program control
- Granularity: Least significant bit represents 1/1024 second; others on request.
- Interrupt: Interrupt occurs when program preset value is reached.

Synchronizer
- Interrupt: Interrupt occurs whenever the non-I/O synchronizing control line is set to logical one by an external device.
- Purpose: To allow a variable-granularity clock function or to provide a high priority alarm recognition capability.

ARITHMETIC

Organization: 18-bit parallel, one's complement, integer

Execution Times: Typical execution times, including instruction and data fetch plus indexing.

Add, Subtract (single length)	4 *u*sec
Multiply/Divide	14 *u*sec
Add, Subtract (double length)	6 *u*sec
Compare/Masked Compare and Branch	6 *u*sec

Register shifts: right, left, single, double
2+.5n *u*sec (n=shift count)

PHYSICAL

The computer is housed in a single cabinet that contains the power supply, logic circuits, core memory, maintenance and control panel, and a cooling system. Logic modules are encapsulated printed circuit cards which plug into the wired chassis of easily accessible pull-out drawers. The front of each drawer is the associated portion of the computer control panel. The logic and memory drawers are mounted in a vertical position. The power supply drawer is mounted horizontally at the bottom of the cabinet.

Size and Weight

Height: 71.75 inches	Depth: 30.5 inches
Width: 26.25 inches	Weight: 1000+ pounds

Environment
- Operating temperatures 0°C to 50°C
- Non-operating temperatures −62°C to +75°C
- Humidity—Relative humidity to 95 per cent
- Cooling—Blower forced ambient air; water cooling—optional.

Power Requirements
115-volt, ± 5 percent, 3-phase, 400-cps, 2000 watts maximum, air cooled (for 16 I/O channels and 32K memory).

SOFTWARE

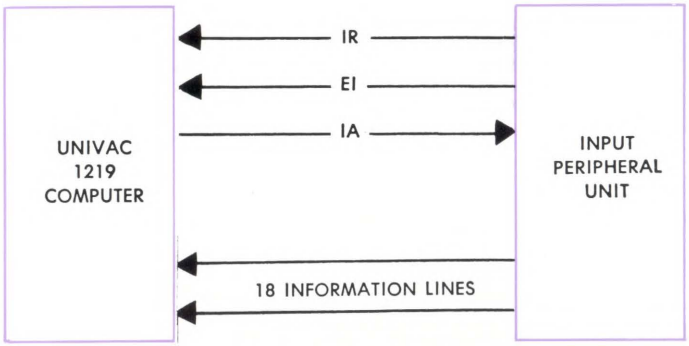
Existing UNIVAC 1218 Operational systems
Mnemonic Assembler TRIM I
Polycode Assemblers TRIM II, TRIM III
Fortran IV
CS-1 Compiler
Floating Point Package
Function Evaluation Routines
Utility Routines
Debugging Routines
Simulators
Diagnostic Routines

CONTROL SIGNALS

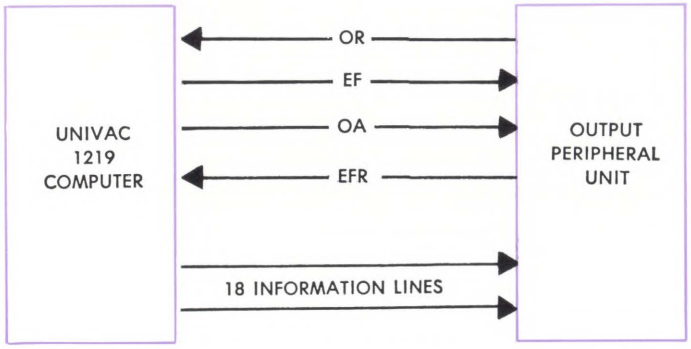
	SIGNAL NAME	ORIGIN	MEANING
Input Channel	Input Request (IR)	Peripheral Equipment	"I have a data word on the input lines ready for you to accept."
	Input Acknowledge (IA)	Computer	"I have sampled the word on the input lines."
	External Interrupt (EI)	Peripheral Equipment	"I have an Interrupt Code word on the input lines ready for you to accept."
Output Channel	Output Request (OR)	Peripheral Equipment	"I am in a condition to accept a word of data from you."
	Output Acknowledge (OA)	Computer	"I have put a data word for you on the output lines; sample them now."
	External Function (EF)	Computer	"I have put an External Function message for you on the output lines; sample them now."
	External Function Request (EFR)	Peripheral Equipment	"I am in a condition to accept an external function message from you."

REGISTERS

ID	SIZE BITS	FUNCTION
AL	18	Accumulator, Lower
AU	18	Accumulator, Upper
SR	5	Special Register
ICR	3	Index Control Register
P	16	Program Address
Sm	16	Storage Address, Main Memory
ZM	18	Storage Transfer, Main Memory
Sc	8	Storage Address, Control Memory
Zc	18	Storage Transfer, Control Memory
D	18	Data Transient
X	18	Exchange Transient
W	18	Auxiliary Arithmetic
CO	18	Output Buffer, Channels 1, 3, 5, 7
CE	18	Output Buffer, Channels O, 2, 4, 6
CO′	18	Output Buffer, Channels 9, 11, 13, 15, (OPT)
CE′	18	Output Buffer, Channels 8, 10, 12, 14 (OPT)
B	18	Data Transient



ONE 1219 INPUT CHANNEL



ONE 1219 OUTPUT CHANNEL

ASSIGNED MEMORY ADDRESS

CONTROL MEMORY (Standard)

Address	Assignment
00000	Fault Interrupt Entrance Register
00001-00010	8 Index Registers
00011	Inter-Computer Time-Out Interrupt Register
00012	Real-Time Clock Interrupt Register
00013	Clock Overflow Interrupt Register
00014	Real-Time Clock Monitor Word Register
00015	Real-Time Clock Incrementing Register
00016	Synchronizing Interrupt Register
00017	Scale Factor Shift Count
00020-00037	Continuous Data Mode (Channels 0-7)
00040-00057	Output Buffer Control Registers (Channels 0-7)
00060-00077	Input Buffer Control Registers (Channels 0-7)

Optional with UNIVAC 1219 Computers equipped with 16 I/O Channels:

00200-00217	UNASSIGNED
00220-00237	Continuous Data Mode (Channels 8-15)
00240-00257	Output Buffer Control Registers (Channels 8-15)
00260-00277	Input Buffer Control Registers (Channels 8-15)

MAIN MEMORY

00100-00117	External Interrupt Registers (Channels 0-7)
00120-00137	UNASSIGNED
00140-00157	Output Monitor Registers (Channels 0-7)
00160-00177	Input Monitor Registers (Channels 9-7)
00300-00317	External Interrupt Registers (Channels 8-15)
00320-00337	UNASSIGNED
00340-00357	Output Monitor Registers (Channels 8-15)
00360-00377	Input Monitor Registers (Channels 8-15)
00400-00477*	UNASSIGNED
00600-00677*	UNASSIGNED
00540-177777	UNASSIGNED

NONDESTRUCTIVE READOUT MEMORY

00500-00537	Bootstrap Program (initial input routine)

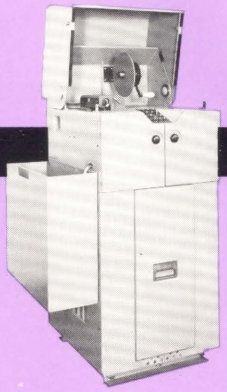
*These addresses are in control memory when 256 words of control memory are used.

UNIVAC 1219 COMPUTER REPERTOIRE OF INSTRUCTIONS

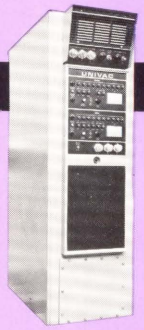
CODE	SYMBOL	DESCRIPTION	TIME μS
02	CMAL	Compare Y	4
03	CMALB	Compare Y+B	4
04	SLSU	Selective Substitute	4
05	SLSUB	Selective Substitute Y+B	4
06	CMSK	Masked Compare Y	4
07	CMSKB	Masked Compare Y+B	4
10	ENTAU	Enter AU, Y	4
11	ENTAUB	Enter AU, Y+B	4
12	ENTAL	Enter AL, Y	4
13	ENTALB	Enter AL, Y+B	4
14	ADDAL	Add Y, 18 bit	4
15	ADDALB	Add Y+B, 18 bit	4
16	SUBAL	Subtract Y, 18 bit	4
17	SUBALB	Subtract Y+B, 18 bit	4
20	ADDA	Add Y, 36 bit	6
21	ADDAB	Add Y+B, 36 bit	6
22	SUBA	Subtract Y, 36 bit	6
23	SUBAB	Subtract Y+B, 36 bit	6
24	MULAL	Multiply Y	14
25	MULALB	Multiply Y+B	14
26	DIVA	Divide, Y	14
27	DIVAB	Divide, Y+B	14
30	IRJP	Indirect RJP, Y	6
31	IRJPB	Indirect RJP, Y+B	6
32	ENTB	Enter B, Y	4
33	ENTBB	Enter B, Y+B	4
34	JP	Jump, Y	2
35	JPB	Jump, Y+B	2
36	ENTBK	Enter, B, U	2
37	ENTBKB	Modify B, U	2
40	CL	Store Zero, Y	4
41	CLB	Store Zero, Y+B	4
42	STRB	Store, B, Y	4
43	STRBB	Store B, Y+B	4
44	STRAL	Store AL, Y	4
45	STRALB	Store AL, Y+B	4
46	STRAU	Store AU, Y	4
47	STRAUB	Store AU, Y+B	4
51	SLSET	Selective Set (IOR), Y	4
52	SLCL	Selective Clear (AND), Y	4
53	SLCP	Selective Complement (XOR), Y	4
54	IJPEI	Indirect Jump (RIL), Y	4
55	IJP	Indirect Jump, Y	4
56	BSK	Increment B, Skip, Y	4
57	ISK	Decrement Index, Skip, Y	6
60	JPAUZ	Jump AU Zero, Y	2
61	JPALZ	Jump AL Zero, Y	2
62	JPAUNZ	Jump AU Not Zero, Y	2
63	JPALNZ	Jump AL Not Zero, Y	2
64	JPAUP	Jump AU Positive, Y	2
65	JPALP	Jump AL Positive, Y	2
66	JPAUNG	Jump AU Negative, Y	2
67	JPALNG	Jump AL Negative, Y	2
70	ENTALK	Enter AL, Y	2
71	ADDALK	Add U, 12 bits	2
72	STRICR	Store ICR, Y	4
73	BJP	Decrement B, Jump, Y	2
74	STRADR	Store Address, Y	4
75	STRSR	Store SR, Deactivate SR, Y	4
76	RJP	Return Jump, Y	4
5001	SIN	Set Input Active	2
5002	SOUT	Set Output Active	2
5003	SEXF	Set External Function Active	2
5011	IN	Initiate Input Buff, k	6
5012	OUT	Initiate Output Buff, k	6
5013	EXF	External Function	6
5014	RTC	Enable Real-Time Clock	2
5015	INSTP	Terminate Input, k	2
5016	OUTSTP	Terminate Output, k	2
5017	EXFSTP	Terminate External Function, k	2
5020	SRSM	Set Resume ff (Intercomp)	2
5021	SKPIIN	Skip Input Inact, k	2
5022	SKPOIN	Skip Output Inact, k	2
5023	SKPFIN	Skip on Ext. Fnct. Inact.	2
5024	WTFI	Wait for Interrupt	2
5026	OUTOV	Force Output One Word, k	2
5027	EXFOV	Force Ext Function One Word, k	2
5030	RIL	Remove Interrupt Lockout	2
5032	EXL	Remove Ext Interrupt Lockout	2
5034	SIL	Set Interrupt Lockout	2
5036	SXL	Set Ext Interrupt Lockout	2
5041	RSHAU	Right Shift AU, k	4-10
5042	RSHAL	Right Shift AL, k	4-10
5043	RSHA	Right Shift A, k	4-20
5044	SF	Scale A Left, k, SF	4-20
5045	LSHAU	Left Shift AU, k	4-10
5046	LSHAL	Left Shift AL, k	4-10
5047	LSHA	Left Shift A, k	4-20
5050	SKP	Skip Console Key, k	2
5051	SKPNBO	Skip No Borrow	2
5052	SKPOV	Skip Overflow	2
5053	SKPNOV	Skip No Overflow	2
5054	SKPODD	Skip L(AU, AL) Odd Parity	2
5055	SKPEVN	Skip L(AU, AL) Even Parity	2
5056	STOP	Stop Console Key, k	2
5057	SKPNR	Skip No Resume ff (Intercomp)	2
5060	RND	Round AU	2
5061	CPAL	Complement AL	2
5062	CPAU	Complement AU	2
5063	CPA	Complement A	2
5072	ENTICR	Enter ICR, k	2
5073	ENTSR	Enter, SR, k	2

PERIPHERAL DEVICES

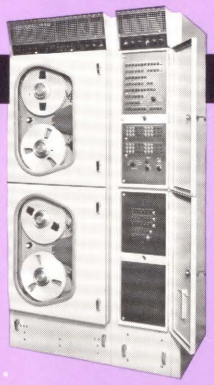
INPUT/OUTPUT CONSOLE



PAPER TAPE UNIT



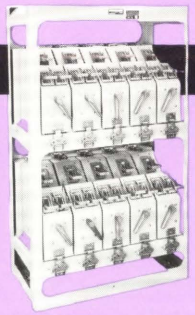
DATA TRANSMISSION UNIT



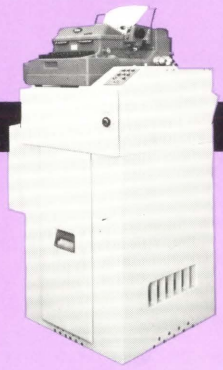
MAGNETIC
TAPE UNIT

TELETYPEWRITER SET

LINE PRINTER



INTERCONNECTION PANEL



MONITORING TYPEWRITER

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